



UNIVERSITY OF MINES AND TECHNOLOGY, TARKWA

SECOND SEMESTER EXAMINATIONS, MAY 2018

COURSE NO: CE 172 Unihubgh.com
COURSE NAME: COMP. ARCHITECTURE & ORGANISATION
CLASS: CE I TIME: 3 HOURS

Name: _____ Index Number: _____

INSTRUCTIONS: Attempt **All QUESTIONS** in SECTIONS A, SECTION B and **Two (2) QUESTIONS** in SECTION C. You are advised not to spend more than 1 hour on SECTION A.

SECTION A

Answer on the question paper by circling or ticking (✓) the correct answers. Each question carries **0.5 Mark**. An incorrect answers attracts a **-0.5 Mark**, so do not guess OR copy.

1. The reason for the implementation of the cache memory is _____
 - a) To increase the internal memory of the system
 - b) The difference in speeds of operation of the processor and memory
 - c) To reduce the memory access and cycle time
 - d) All of the mentioned

2. The _____ format is usually used to store data.
 - a) BCD
 - b) Decimal
 - c) Hexadecimal
 - d) Octal

3. During the execution of a program which gets initialized first?
 - a) MDR
 - b) IR
 - c) PC
 - d) MAR

4. The effectiveness of the cache memory is based on the property of _____
- a) Locality of reference
 - b) Memory localization
 - c) Memory size
 - d) None of the mentioned
5. A source program is usually in _____
- a) Assembly language
 - b) Machine level language
 - c) High-level language
 - d) Natural language
6. The correspondence between the main memory blocks and those in the cache is given by _____
- a) Hash function
 - b) Mapping function
 - c) Locale function
 - d) Assign function
7. The control unit controls other units by generating _____
- a) Control signals
 - b) Timing signals
 - c) Transfer signals
 - d) Command Signals
8. The write-through procedure is used
- a) To write onto the memory directly
 - b) To write and read from memory simultaneously
 - c) To write directly on the memory and the cache simultaneously
 - d) None of the mentioned

9. Which memory device is generally made of semi-conductors?

- a) RAM
- b) Hard-disk
- c) Floppy disk
- d) Cd disk

10. The decoded instruction is stored in _____

- a) IR
- b) PC
- c) Registers
- d) MDR

11. The registers, ALU and the interconnection between them are collectively called as _____

- a) process route
- b) information trail
- c) information path
- d) data path

12. Pipe-lining is a unique feature of _____

- a) RISC
- b) CISC
- c) ISA
- d) IANA

13. The instruction, Add #45, R1 does _____

- a) Adds the value of 45 to the address of R1 and stores 45 in that address
- b) Adds 45 to the value of R1 and stores it in R1
- c) Finds the memory location 45 and adds that content to that of R1
- d) None of the mentioned

14. In case of, Zero-address instruction method the operands are stored in _____

- a) Registers
- b) Accumulators
- c) Push down stack
- d) Cache

15. The smallest entity of memory is called as _____

- a) Cell
- b) Block
- c) Instance
- d) Unit

16. If a system is 64-bit machine, then the length of each word will be _____

- a) 4 bytes
- b) 8 bytes
- c) 16 bytes
- d) 12 bytes

17. The type of memory assignment used in Intel processors is _____

- a) Little Endian
- b) Big Endian
- c) Medium Endian
- d) None of the mentioned

18. When using the Big-Endian assignment to store a number, the sign bit of the number is stored in _____

- a) The higher order byte of the word
- b) The lower order byte of the word
- c) Can't say
- d) None of the mentioned

19. The main aim of virtual memory organisation is

- a) To provide effective memory access
- b) To provide better memory transfer

- c) To improve the execution of the program
d) All of the mentioned

20. The addressing mode/s, which uses the PC instead of a general-purpose register is _____

- a) Indexed with offset
b) Relative
c) Direct
d) both Indexed with offset and direct

21. The fastest data access is provided using _____

- a) Caches
b) DRAM's
c) SRAM's
d) Registers

22. The signal sent to the device from the processor to the device after receiving an interrupt is

- a) Interrupt-acknowledge
b) Return signal
c) Service signal
d) Permission signal

23. When the process is returned after an interrupt service _____ should be loaded again.

- i. Register contents
ii. Condition codes
iii. Stack contents
iv. Return addresses

- a) i,iv
b) ii,iii and iv
c) iii,iv
d) i,ii

24. The time between the receipt of an interrupt and its service is _____

- a) Interrupt delay
- b) Interrupt latency
- c) Cycle time
- d) Switching time

25. The PC gets incremented

- a) After the instruction decoding
- b) After the IR instruction gets executed
- c) After the fetch cycle
- d) None of the mentioned

26. _____ converts the programs written in assembly language into machine instructions.

- a) Machine compiler
- b) Interpreter
- c) Assembler
- d) Converter

27. The method of mapping the consecutive memory blocks to consecutive cache blocks is called _____

- a) Set associative
- b) Associative
- c) Direct
- d) Indirect

28. In associative mapping, in a 16-bit system the tag field has _____ bits.

- a) 12
- b) 8
- c) 9
- d) 10

29. The main virtue for using single Bus structure is _____

- a) Fast data transfers
- b) Cost effective connectivity and speed
- c) Cost effective connectivity and ease of attaching peripheral devices
- d) None of the mentioned

30. Which method/s of representation of numbers occupies large amount of memory than others?

- a) Sign-magnitude
- b) 1's compliment
- c) 2's compliment
- d) 1's & 2's compliment

31. When we perform subtraction on -7 and 1 the answer in 2's compliment form is _____

- a) 1010
- b) 1110
- c) 0110
- d) 1000

32. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

- a) A
- b) B
- c) Both take the same time
- d) Insufficient information

33. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____

- a) Super-scaling
- b) Pipe-lining
- c) Parallel Computation
- d) None of the mentioned

34. In memory-mapped I/O _____

- a) The I/O devices and the memory share the same address space
- b) The I/O devices have a separate address space
- c) The memory and I/O devices have an associated address space
- d) A part of the memory is specifically set aside for the I/O operation

35. To overcome the lag in the operating speeds of the I/O device and the processor we use

- a) Buffer spaces
- b) Status flags
- c) Interrupt signals
- d) Exceptions

36. The method of accessing the I/O devices by repeatedly checking the status flags is

- a) Program-controlled I/O
- b) Memory-mapped I/O
- c) I/O mapped
- d) None of the mentioned
- e)

37. The number successful accesses to memory stated as a fraction is called as _____

- a) Hit rate
- b) Miss rate

c) Success rate

d) Access rate

38. In associative mapping during LRU, the counter of the new block is set to '0' and all the others are incremented by one, when _____ occurs.

a) Delay

c) Hit

b) Miss

d) Delayed hit

39. The DMA differs from the interrupt mode by

a) The involvement of the processor for the operation

b) The method accessing the I/O devices

c) The amount of data transfer possible

d) None of the mentioned

40. The DMA transfer is initiated by _____

a) Processor

c) I/O devices

b) The process being executed

d) OS

[20 marks]

SECTION B

Indicate in the spaces provided whether the sentences or statements are **TRUE** or **FALSE**

1. The entire computer system is coordinated by the CPU? _____
2. The SIM is a type of memory. _____
3. MAR is the register containing addresses in memory. _____
4. The peripherals constitute part of the computer system. _____
5. Instructions in a program memory are generally executed in random order.

6. Cache is the fastest small memory. _____
7. If we use the flash drives instead of the hard disks, then the secondary storage can go above primary memory in the hierarchy. _____
8. In the memory hierarchy, as the speed of operation increases the memory size also increase. _____
9. In direct mapping the presence of the block in memory is checked with the help of block field. _____
10. The associative mapping is costlier than direct mapping technique. _____
11. In Intel's IA-32 architecture there is a separate 16-bit address space for the I/O devices? _____
12. The directly mapped cache no replacement algorithm is required? _____
13. In double precision format the size of the mantissa is 32-bit? _____
14. The interrupt-request line is a part of the control line. _____
15. A single interrupt line can be used to service n different devices? _____

16. The physical memory is not as large as the address space spanned by the processor.

17. The DMA doesn't make use of the MMU for bulk data transfers. _____

18. The only difference between the EEPROM and flash memory is that the latter doesn't allow bulk data to be written. _____

19. The memory allocated to each page are contiguous? _____

20. The type of memory assignment used in Intel processor is Big endian.

[20 marks]

SECTION C

Answer ONLY TWO (2) QUESTIONS. QUESTION ONE is Compulsory

QUESTION ONE

a.

I. Define Paging

[3 marks]

II. Explain Register Addressing mode of a processor?

[3 mark]

III. State Amdahl's law.

[3 marks]

b.

I. What is ISR?

[3 mark]

II. State the four (4) main primary function of the CPU.

[4 marks]

I. Find the CPI for the program.

[10 marks]

II. If the number of load instructions can be reduced to one half of that of Arithmetic instructions, what is the speedup and the new CPI?

[10 marks]

b. Provide the set of instructions to compute the operation given below using a 3-address instruction format.

$$X = 2K(A+B) - C(D-2E) + 2Q(4 - 2C)$$

[7 Marks]

c. The following table shows pairs of hexadecimal numbers.

A	B
14F6	672F

I. What is the sum of A and B if they represent unsigned 16-bit hexadecimal numbers? The result should be written in hexadecimal. Show your work.

[5 Marks]

II. What is the sum of A and B if they represent signed 16-bit hexadecimal numbers stored in sign-magnitude format? The result should be written in hexadecimal. Show your work.

[8 marks]

Examiners: T. Kwantwi