



# UNIVERSITY OF MINES AND TECHNOLOGY, TARKWA

FIRST SEMESTER EXAMINATIONS, NOV/DEC 2018

COURSE NO: CE 471

COURSE NAME: INDUSTRIAL ELECTRONIC

CLASS: CE IV

TIME: 3 HOURS

Name: \_\_\_\_\_ Index Number: \_\_\_\_\_

## ATTEMPT ALL QUESTIONS

### QUESTION 1.

[40 Marks]

- (a) (i) What are the advantages and disadvantages of silicon control rectifier  
(ii) Draw a full-wave rectifier using two (2) SCRs and explain its operation  
(iii) The gate current in a thyristorised full-wave rectifier is adjusted to 1.2 mA and the forward breakdown voltage of SCR corresponding to this gate current is 150 V. The applied voltage is a sinusoidal voltage of 300 V peak, the load resistance is 100  $\Omega$  and the holding current is zero. Determine (i) firing angle (ii) conduction angle (iii) average output voltage (iv) average current and (v) power output.
- (b) For the UJT relaxation oscillator in figure 1 below, it is known that  $R_{BB} = 5K\Omega$ ,  $\eta = 0.6$ ,  $V_V = 1 V$ ,  $I_V = 10 mA$ ,  $I_P = 10\mu A$ , and  $R_{B1} = 100\Omega$  during discharge stage. Determine;  
(i) The value of  $V_P$  to switch-on the UJT;  
(ii) The range of  $R_1$  to switch-on and switch-off the UJT;  
(iii) Frequency of oscillation if  $R_{B1} = 100\Omega$  during discharge phase of the capacitor  $C$ ;  
(iv) Sketch the wave shape of  $V_C$  and  $V_{R2}$ .

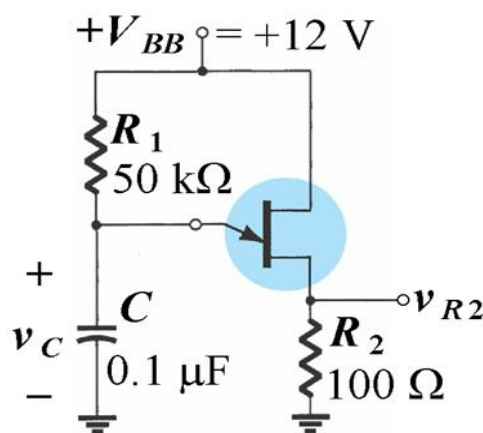


Figure 1

**QUESTION 2****[30 Marks]**

- (a) (i) State the merits and limitations of digital techniques  
 (ii) The output  $V_0$  of an N-bit D/A converter is given by:

$V_0 = (2^{N-1}a_{N-1} + 2^{N-2}a_{N-2} + \dots + 2^2a_2 + 2^1a_1 + a_0)K$  ; Where K is a proportionality factor determined by the system parameters and where the coefficient  $a_j$  represent the binary word and  $a_j = 1(0)$  if the jth bit is 1(0). A 6 bit D/A converter gives  $V_0 = 7.2$  V for the word 100100. Find the value of  $V_0$  for the word 110011.

- (ii) For the R-2R ladder D/A converter shown in fig. 2, find the value of the output voltage  $V_0$  when  $V_{REF} = 12$  V. Clearly show the steps in your calculations.

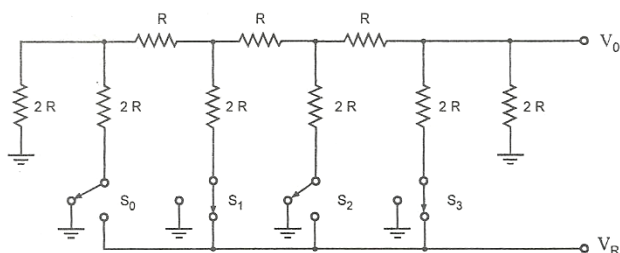


Fig. 2

- (b) Define  
 (i) The lock range  
 (ii) The capture range  
 (iii) Pull in time  
 (iv) Determine the free running frequency, the lock range and capture range for an NE/SE 565 phase lock loop if  
 $V^+ = 12$  V;  $V^- = -12$  V;  $R_1 = 15$  k $\Omega$ ,  $C_1 = 0.01$   $\mu$ F and  $C_2 = 10$   $\mu$ F.

**QUESTION 3****[30 Marks]**

- (a) Draw the block diagram of a basic Cathode Ray Oscilloscope and explain each block.  
 (b) Implement the sum -of- products of the Boolean function expressed by  $f(A, B, C) = \sum m(0,3,4,6,7)$  with a suitable multiplexer using C as one of the inputs.

*Examiner: E. Addo*